IN THE SPECIFICATION

Please replace paragraph beginning on page 3, line 31 with the following amended paragraph:

The filtering circuit is based on a differential pair made up of NMOS-type transistors 101 and 102 whose gates constitute inputs IN1 and IN2 and receive the differential signal to be filtered. The source of each of NMOS-type transistors 101 and 102 is connected to the drain of an NMOS-type transistor 105, which is used as power source for the differential pair. Transistor 105 has a source electrode connected to a first reference voltage, such as, ground. The drain of transistor 101 (respectively 102) is connected to the drain of a PMOS-type transistor 103 (respectively 104) whose source is connected to supply voltage V_{dd}. The drain of transistor ~~105~~ 103 (respectively 104) is connected to a first output OUT_1 (respectively second output OUT_2). The gates of transistors 103 and 104 are connected to the gate of a PMOS-type transistor 107 that has a source connected to a second reference voltage, such as supply voltage V_{dd}. Transistor 107 has a drain connected to the drain and the gate of an NMOS-type transistor 108, and to the gate of transistor 105 that is the power source for the differential pair 101 and 102. The source of transistor 108 is connected to the ground level of the circuit.